

Electrical Engineering Department

Superconducting Fault Current Limiters

UNINOVA – Centre of Technology and Systems



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Objectives

- Development of methodologies and simulations of inductive superconducting fault current limiters, allowing to analyze its performance in power grids with different degrees of complexity, and thus contributing to the advent of sustainable technologies based on superconducting materials.
- Collaboration on tasks of R&D in a 15 kV real prototype.

Methodology

- Conduct a comprehensive literature review on the problems associated with the increasing penetration of distributed generation and how the superconducting technology can mitigate these problems, with special focus on current limiting superconducting inductive type (see Fig. 1).
- Develop a methodology to design inductive limiters with secondary second-generation tape (see Fig. 2 and Fig. 3), a topology under patent by the host institution.
- Design a device to a network of 400 V/100 A (see Fig. 4) and carrying out experimental tests.

Expected Results

- Validation of simulations by collected data from laboratory tests, allowing the development of a tool or module that can be integrated into a network simulation software.
- Lowering fault current levels and reduced AC losses on modern power grids by adding such limiters.
- Scale the laboratory device to a full device to work in real environment.

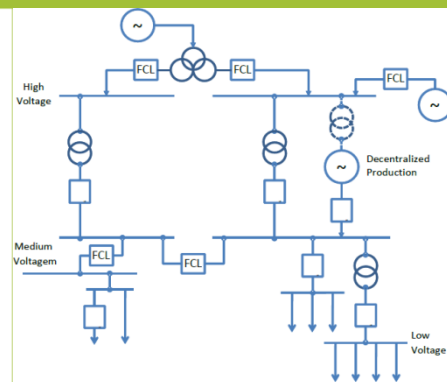


Fig. 1 – Possible location of fault current limiters in the power grid.

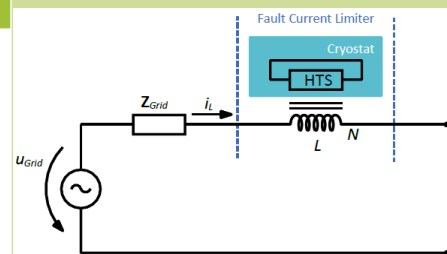


Fig. 2 – Inductive fault current limiter principle.

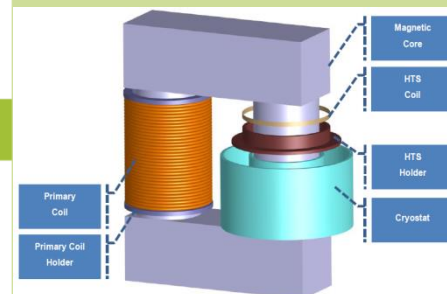


Fig. 3 – Inductive fault current limiter components.

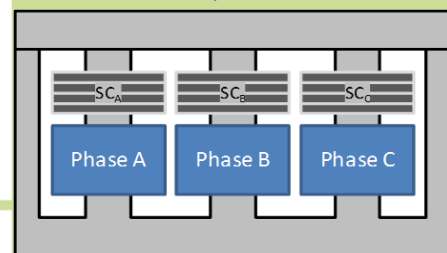


Fig. 4 – Inductive fault current limiter scheme for a three-phase power grid.