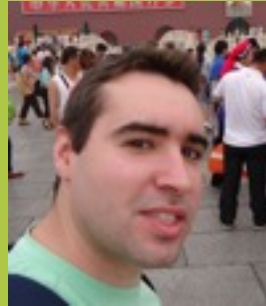


Transactional Memory Verification

COMPUTER SYSTEMS / CR4 Team



Ricardo Dias

PhD Student / Supervised by:
Prof. João Lourenço

Currently working on compiler and runtime support for software transactional memory using automatic verification techniques.

Objectives

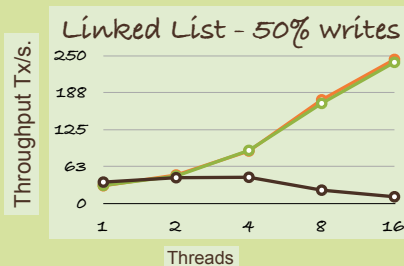
- Improving resource utilization in modern multi-core computers
- Providing software developers with new techniques and tools for parallel and distributed computing
- Enabling High-Performance Computing for a broader community of researchers and industry
- Improving the productivity of applications deployed in the Cloud

Methodology

- Use Transactional Memory Paradigm
- Advance the state-of-the-art in transactional memories
- Development of mathematical models and computational prototypes
- Validation process includes running experimental tests
- Evaluation includes comparison with similar state-of-the-art approaches

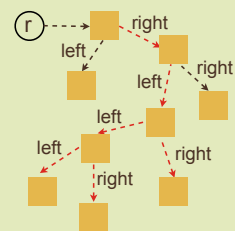
Expected Results

- Contribute to more efficient computing
- Bring parallel programming to the masses
- Advance the state-of-the-art in transactional memories
- Prototype that allows to scale applications to computer clusters and/or the Cloud



Heap Program Verification

Tree-based Data Structures



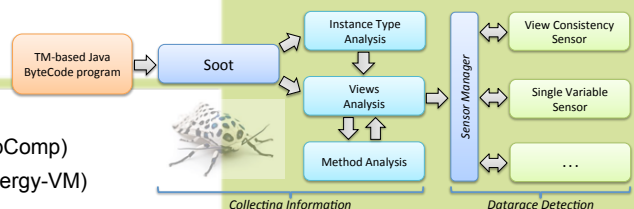
Separation Logic Representation

$$\text{tree}(r) \Leftrightarrow r = \text{nil} \wedge \exists l', r'. r \rightarrow [\text{left}:l', \text{right}:r'] * \text{tree}(l') * \text{tree}(r')$$

Heap Path Expressions

$$r.\text{right}.\text{left}.\text{(left | right)}^*$$

Atomicity Violations Detection



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PTDC/EIA-EIA/113613/2009 (Synergy-VM)

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Collecting Information

Data Race Detection